AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method, comprising:

receiving accelerated graphics port (AGP) transaction requests at a first bus interface from a core logic device, and transmitting the AGP transaction requests to the core logic device;

buffering the received AGP transaction requests using a request queue coupled to the first bus interface;

exchanging the AGP transaction requests using a second bus interface for access to the first bus interface between the core logic device and a graphics controller; and

arbitrating access to the first bus interface using a request arbiter coupled to the second bus interface.

2. (Original) The method of claim 1, further comprising:

initiating data transactions by the graphics controller, and receiving data transactions initiated by the core logic device using a third bus interface;

exchanging the AGP transaction requests for access to the second bus interface between the core logic device and the graphics controller; and

arbitrating access to the second bus interface using a data transaction arbiter coupled to the third bus interface.

3. (Original) The method of claim 2, further comprising:

initiating data transactions by the graphics controller, and receiving data transactions initiated by the core logic device using a fourth bus interface;

exchanging the AGP transaction requests for access to the third bus interface between the core logic device and the graphics controller; and

arbitrating access to the third bus interface using a data transaction arbiter coupled to the fourth bus interface.

4. (Original) The method of claim 1, further comprises implementing a common, distributed arbitration mechanism using the request arbiter and a corresponding request arbiter of the core logic device.

5. (Currently Amended) A system, comprising:

a storage medium;

a processor coupled with the storage medium; and

a graphics controller coupled to the storage medium and the processor, the graphics controller having

a first bus interface to receive accelerated graphics port (AGP) transaction requests from a core logic device, and to transmit the AGP transaction requests to the core logic device,;

a request queue coupled to the first bus interface to buffer received AGP transaction requests,;

a second bus interface to exchange requests for access to the first bus interface between the core logic device and a graphics controller,; and

a request arbiter coupled to the second bus interface to arbitrate access to the first bus interface.

6. (Original) The system of claim 5, wherein the graphic controller further comprising:

a third bus interface to initiate data transactions by the graphics controller and to receive data transactions initiated by the core logic device;

a fourth bus interface to exchange requests for access to the third bus interface between the core logic device and the graphics controller; and

a data transaction arbiter coupled to the fourth bus interface to arbitrate access to the fourth bus interface.

7. (Original) The system of claim 6, wherein the request arbiter of the core logic device is to implement a common, distributed arbitration mechanism.

8. (Currently Amended) A graphics controller, comprising:

a first bus interface to receive accelerated graphics port (AGP) transaction requests from a core logic device, and to transmit the AGP transaction requests to the core logic device;

a request queue coupled to the first bus interface to buffer received AGP transaction requests;

a second bus interface to exchange requests for access to the first bus interface between the core logic device and a graphics controller; and

a request arbiter coupled to the second bus interface to arbitrate access to the first bus interface.

9. (Original) The graphics controller of claim 8, further comprising:

a third bus interface to initiate data transactions by the graphics controller and to receive data transactions initiated by the core logic device;

a fourth bus interface to exchange requests for access to the third bus interface between the core logic device and the graphics controller; and

a data transaction arbiter coupled to the fourth bus interface to arbitrate access to the fourth bus interface.

10. (Original) The graphics controller of claim 8, wherein the request arbiter of the core logic device is to implement a common, distributed arbitration mechanism.

Claims 11–18 (Cancelled)

19. (New) The method of claim 1, wherein the core logic device and the graphics controller function as a single virtual graphics controller.

20. (New) The system of claim 5, wherein the core logic device and the graphics controller function as a single virtual graphics controller.

21. (New) The graphics controller of claim 8, wherein the core logic device and the graphics controller function as a single virtual graphics controller.

22. (New) A machine-readable medium having stored thereon data representing sets of instructions which, when executed by a machine, cause the machine to:

receive accelerated graphics port (AGP) transaction requests at a first bus interface from a core logic device, and transmit the AGP transaction requests to the core logic device;

buffer the received AGP transaction requests using a request queue coupled to the first bus interface;

exchange the AGP transaction requests using a second bus interface for access to the first bus interface between the core logic device and a graphics controller; and

arbitrate access to the first bus interface using a request arbiter coupled to the second bus interface.

23. (New) The machine-readable medium of claim 22, wherein the sets of instructions which, when executed by the machine, further cause the machine to:

initiate data transactions by the graphics controller, and receive data transactions initiated by the core logic device using a third bus interface;

exchange the AGP transaction requests for access to the second bus interface between the core logic device and the graphics controller; and

arbitrate access to the second bus interface using a data transaction arbiter coupled to the third bus interface.

24. (New) The machine-readable medium of claim 23, wherein the sets of instructions which, when executed by the machine, further cause the machine to:

initiate data transactions by the graphics controller, and receive data transactions initiated by the core logic device using a fourth bus interface;

exchange the AGP transaction requests for access to the third bus interface between the core logic device and the graphics controller; and

arbitrate access to the third bus interface using a data transaction arbiter coupled to the fourth bus interface.

25. (New) The machine-readable medium of claim 22, wherein the sets of instructions which, when executed by the machine, further cause the machine to implement a common, distributed arbitration mechanism using the request arbiter and a corresponding request arbiter of the core logic device.

26. (New) The machine-readable medium of claim 22, wherein the core logic device

and the graphics controller function as a single virtual graphics controller.